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| **18EES101J-BASIC ELECTRICAL AND ELECTRONICS ENGINEERING (LAB)** |
| **RECORD**  **SEMESTER I**    **ACADEMIC YEAR: 2020-21**  **NAME : *Tambe Utkarsh Yashwant.***  **REG. NO. : *RA2011027010166***  C:\Users\System 1\Desktop\11.png  **DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING**  **FACULTY OF ENGINEERING & TECHNOLOGY**  **SRM INSTITUTE OF SCIENCE AND TECHNOLOGY**  (Formerly SRM University, Under section 3 of UGC Act, 1956)  **S.R.M. NAGAR, KATTANKULATHUR – 603 203**  **KANCHEEPURAM DISTRICT** |



**SRM Institute of Science and Technology**

(Deemed to be University)

**S.R.M. NAGAR, KATTANKULATHUR -603 203**

**KANCHEEPURAM DISTRICT**

**BONAFIDE CERTIFICATE**

**Register No : *RA2011027010166***

Certified to be the bonafide record of work done by *Tambe Utkarsh Yashwant* of *Computer Science & Engineering department*, B.Techdegree course in the Practical of 18EES101J Basic Electrical and Electronics Engineering in **SRM IST, Kattankulathur** during the academic year 2018-2019. **Lab in-charge**

**Date: Year Co-ordinator**

Submitted for end semester examination held in\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Lab, SRMIST**,** Kattankulathur**.**

**Date: Examiner-1 Examiner-2**

**LIST OF EXPERIMENTS**

1. Verification of Kirchhoff’s laws

2. Verification of All Theorems (Thevenin’s theorem, Norton’s theorem, Maximum power transfer theorem)

3. Transient analysis of RL an RC series circuits

4. Load test on single phase transformer

5. Demo of DC/AC machines & Parts

6. Types of wiring (fluorescent lamp wiring, staircase wiring)

7. Characteristics of semiconductor devices (PN junction, Zener diode, BJT)

8. Wave shaping circuits (Half and full wave rectifier, clipper)

9. Displacement measurement using LVDT and pressure measurement using Strain gauge

10. Verification and interpretation of Logic Gates.

11. Reduction of Boolean expression using K-map

12. Study of modulation and demodulation techniques.

**INDEX**

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| --- | --- | --- | --- |
| **Sl. No.** | **Name of the Experiment** | **Marks (50)** | **Signature**  **of the Staff** |
| 1 | **Verification of Kirchhoff’s laws** |  |  |
| 2 | **Verification of All Theorems**  **(Thevenin’s theorem, Norton’s theorem, Maximum power transfer theorem)** |  |  |
| 3 | Transient analysis of RL an RC series circuits |  |  |
| 4 | Load test on single phase transformer |  |  |
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| 11 | Reduction of Boolean expression using K-map |  |  |
| 12 | Study of modulation and demodulation techniques. |  |  |

DEPT. OF ELECTRICAL & ELECTRONICS ENGINEERING

SRM INSTITUTE OF SCIENCE AND TECHNOLOGY, Kattankulathur – 603 203

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| Title of Experiment : **1. Verification of Kirchhoff’s Laws** |
| Name of the candidate : *Tambe Utkarsh Yashwant*.  Register Number : *RA2011027010166*  Date of Experiment : *30th September, 2020* |

|  |  |  |  |
| --- | --- | --- | --- |
| Sl.  No. | Marks Split up | Maximum marks  (50) | Marks obtained |
| 1 | Pre Lab questions | 5 |  |
| 2 | Preparation of observation | 15 |  |
| 3 | Execution of experiment | 15 |  |
| 4 | Calculation / Evaluation of Result | 10 |  |
| 5 | Post Lab questions | 5 |  |
| **Total** | | **50** |  |

Staff Signature

**PRE LAB QUESTIONS**

1. **Define Ohm’s law.**

**Ans :-** *Ohm's law states that the current through a conductor between two points is directly proportional to the voltage across the two points.*

1. **State KCL and KVL.**

**Ans :- 1] KCL:** *The sum of all the currents entering a junction in a circuit is equal to the sum of all the currents leaving it.*

**2] KVL:** *The algebraic sum of all the potential differences along a closed loop in a circuit is zero.*

1. **Define absolute potential and potential difference.**

**Ans :- 1] Absolute Potential:** *The electric condition, that determines the flow of charge from one conductor to other in contact, is the****electric potential.***

**2] Potential Difference:** *Voltage, electric potential difference, electric pressure or electric tension is the difference in electric potential between two points, which is defined as the work needed per unit of charge to move a test charge between the two points.*

1. **What is the difference between mesh and loop?**

**Ans :-** *Loop and mesh both are part of an electrical circuit. The loop is found in**a closed circuit with unique nodes that are no nodes are repeated for than one time. A mesh is a loop that has no other circuit paths inside it.*

1. **What is super-node?**

**Ans:-** *A supernode is a theoretical construct that can be used to solve a circuit. This is done by viewing a*[*voltage*](https://en.wikipedia.org/wiki/Voltage)*source on a wire as a point source voltage in relation to other point voltages located at various nodes in the circuit, each supernode contains two nodes, one non-reference node and another node that may be a second non-reference node or the reference node.*

|  |  |
| --- | --- |
| **Experiment No. 1**  **Date : 30/09/2020** | **VERIFICATION OF KIRCHOFF’S LAWS** |

**Aim:**

To verify Kirchhoff’s current law and Kirchhoff’s voltage law for the given circuit.

**Apparatus Required:**

|  |  |  |  |
| --- | --- | --- | --- |
| Sl.No. | Apparatus | Range | Quantity |
| 1 | RPS (regulated power supply) | (0-30V) | 2 |
| 2 | Resistance | 330Ω, 220Ω 1kΩ | 6 |
| 3 | Ammeter | (0-30mA)MC | 3 |
| 4 | Voltmeter | (0-30V)MC | 3 |
| 5 | Bread Board & Wires | -- | Required |

**Statement:**

**KCL:** The algebraic sum of the currents meeting at a node/junction is equal to zero.

**KVL:** In any closed path / mesh, the algebraic sum of all the voltages is zero.

**Precautions:**

1. Voltage control knob should be kept at minimum position.
2. Current control knob of RPS should be kept at maximum position.

**Procedure for KCL:**

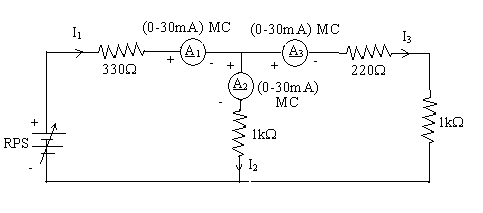
1. Give the connections as per the circuit diagram.
2. Set a particular value in RPS.
3. Note down the corresponding ammeter reading
4. Repeat the same for different voltages

**Procedure for KVL:**

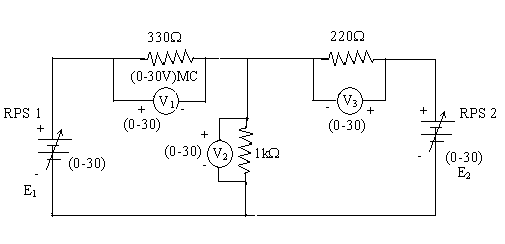
1. Give the connections as per the circuit diagram.
2. Set a particular value in RPS.
3. Note all the voltage reading
4. Repeat the same for different voltages

**HARDWARE SETUP:**

**Circuit for KCL verification:**



**Circuit for KVL verification:**

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**KCL - Theoretical Values:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Sl.  No. | Voltage  E | Current | | | I1 = I2 + I3 |
| I1 | I2 | I3 |
| Volts | mA | mA | mA | mA |
| 1 | 5 | 5 | 3 | 2 | 5 |
| 2 | 10 | 11 | 6 | 5 | 11 |
| 3 | 15 | 17 | 10 | 7 | 17 |
| 4 | 20 |  |  |  |  |
| 5 | 25 |  |  |  |  |

**KCL - Practical Values:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Sl.  No. | Voltage  E | Current | | | I1 = I2 + I3 |
| I1 | I2 | I3 |
| Volts | mA | mA | mA | mA |
| 1 | 5 | 5.68 | 3.12 | 2.56 | 5.68 |
| 2 | 10 | 11.37 | 6.25 | 5.12 | 11.37 |
| 3 | 15 | 17.05 | 9.37 | 7.68 | 17.05 |

**KVL – Theoretical Values**

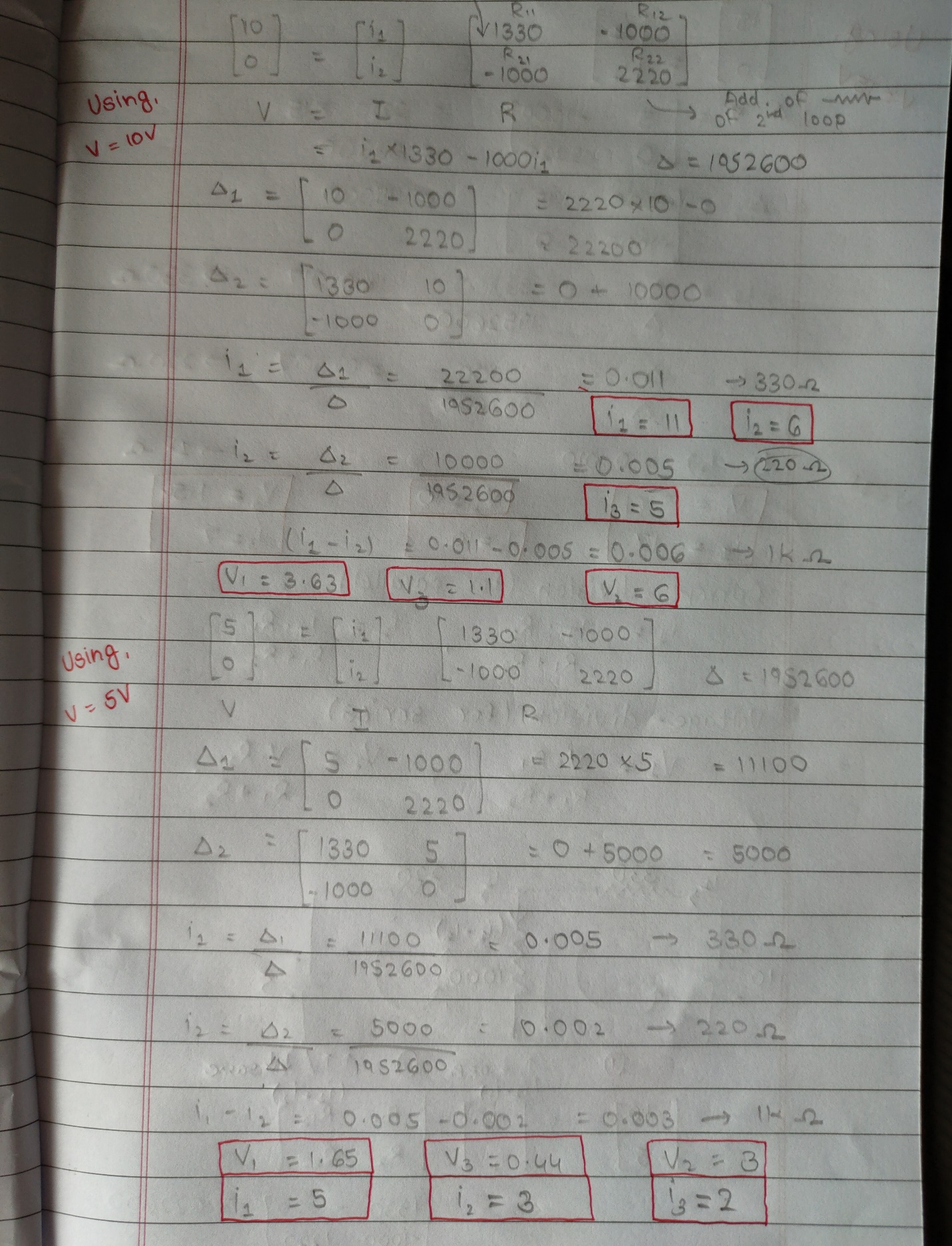
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Sl. No. | RPS | | Voltage | | | KVL  E1 = V1 + V2 |
| E1 | E2 | V1 | V2 | V3 |
| V | V | V | V | V | V |
| 1 | 5 | - | 1.65 | 3 | 0.44 | 4.65 |
| 2 | 10 | - | 3.63 | 6 | 1.1 | 9.63 |
| 3 | 15 | - | 5.61 | 10 | 1.54 | 15.61 |
| 4 | 20 | - |  |  |  |  |
| 5 | 25 | - |  |  |  |  |

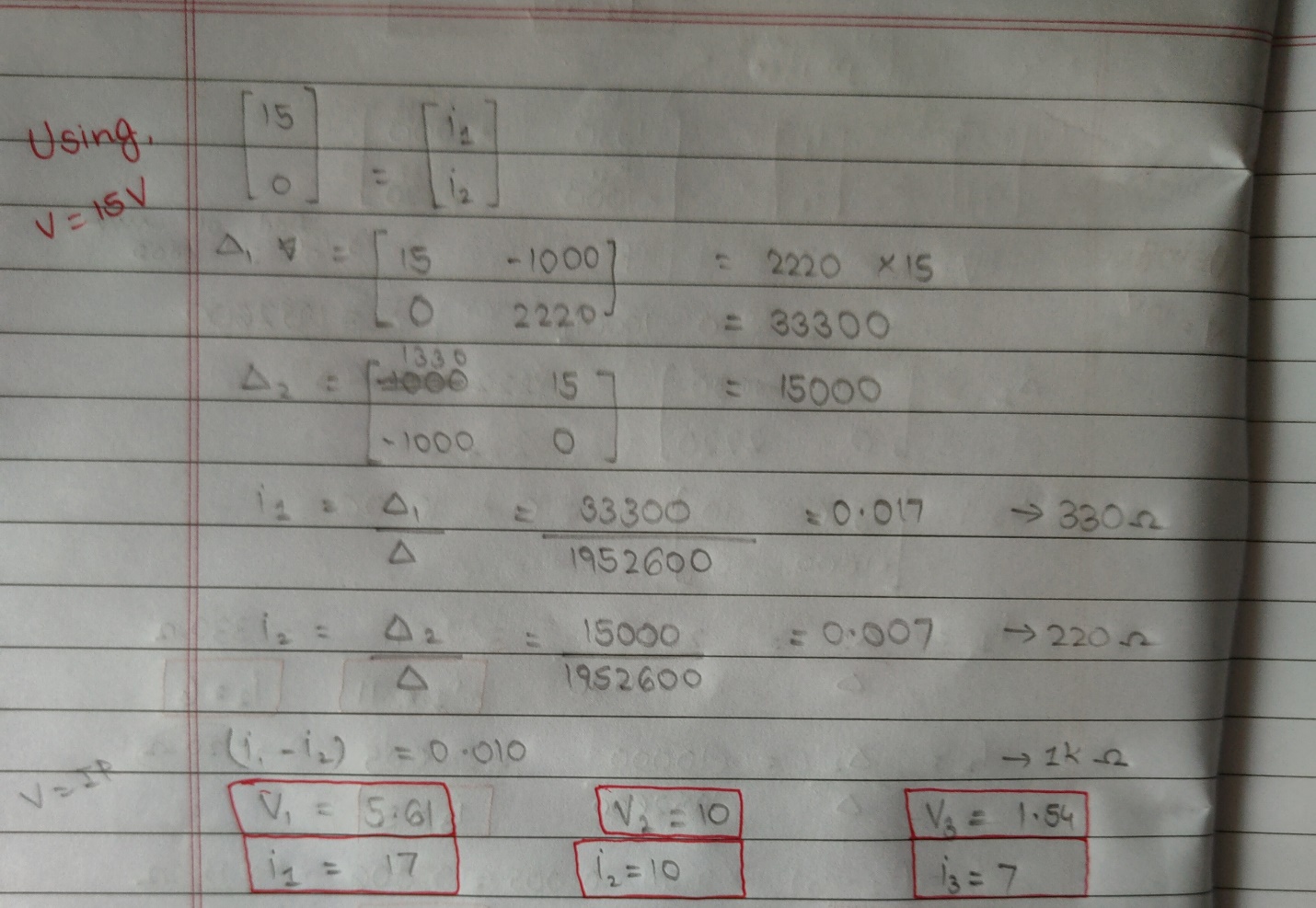
**KVL - Practical Values**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Sl. No. | RPS | | Voltage | | | KVL  E1 = V1 + V2 |
| E1 | E2 | V1 | V2 | V3 |
| V | V | V | V | V | V |
| 1 | 5 | - | 1.88 | 3.12 | 0.56 | 5 |
| 2 | 10 | - | 3.75 | 6.25 | 1.13 | 10 |
| 3 | 15 | - | 5.63 | 9.37 | 1.69 | 15 |

**Model Calculations:**

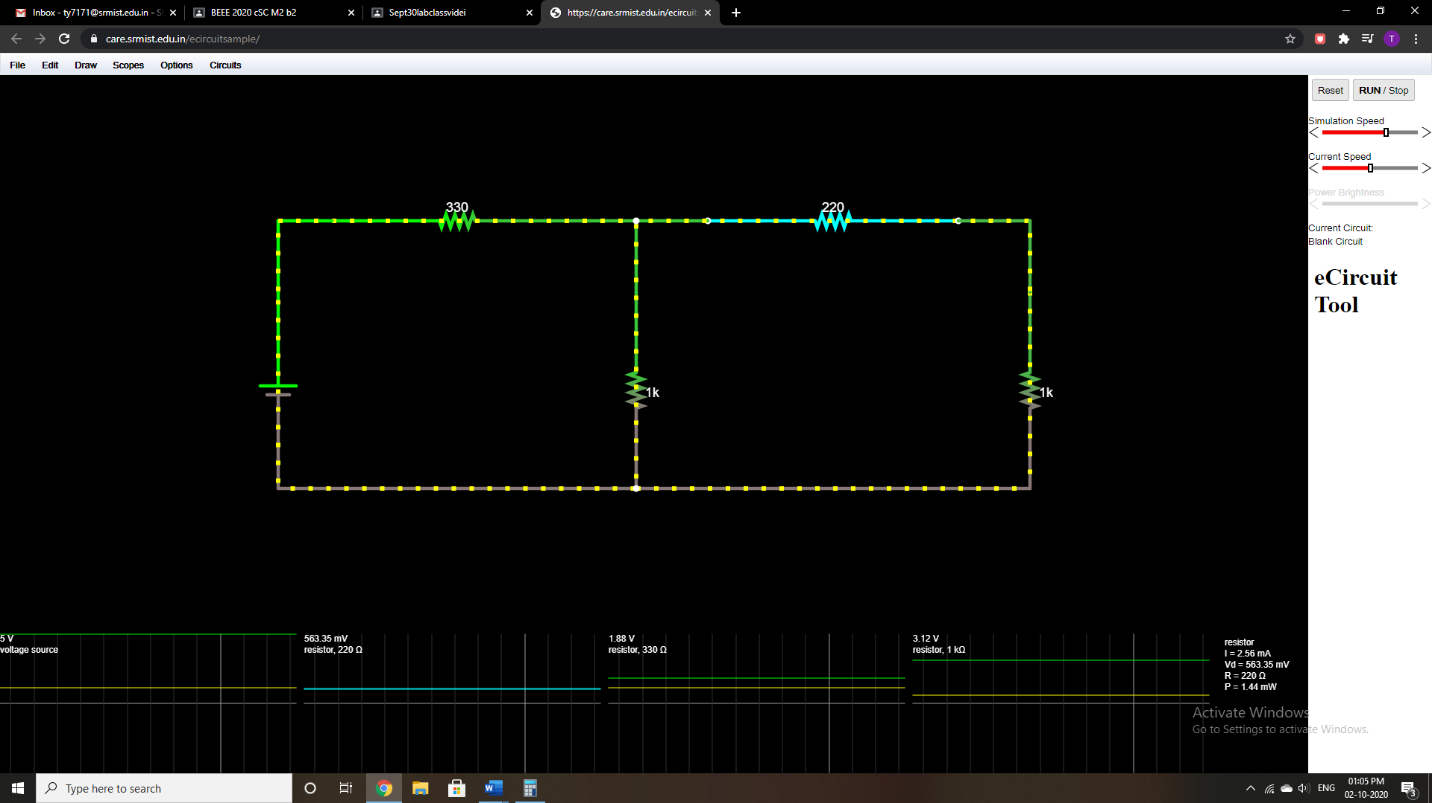
*Model Calcutions are done on Paper & their images are attached on next page…*

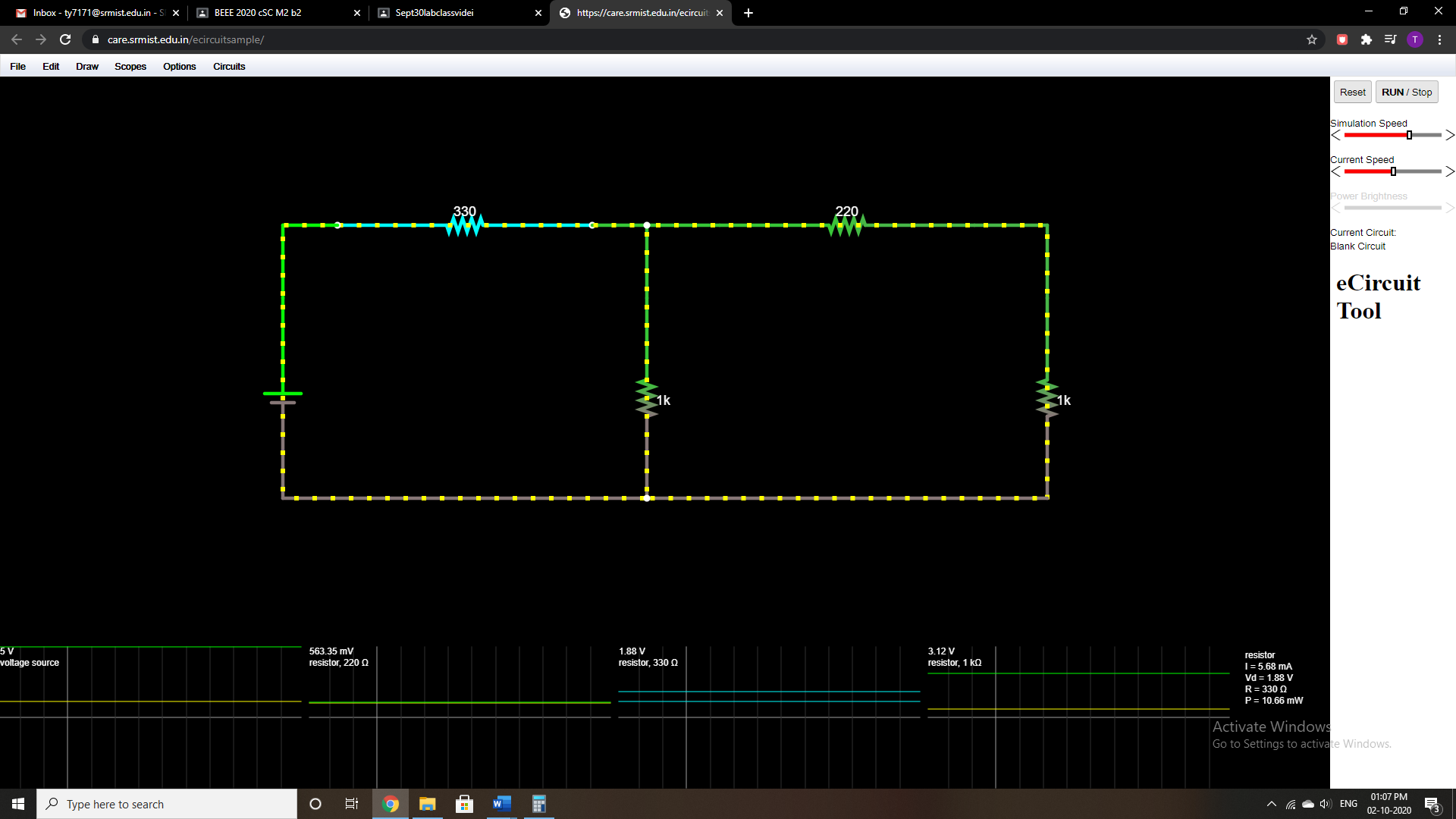
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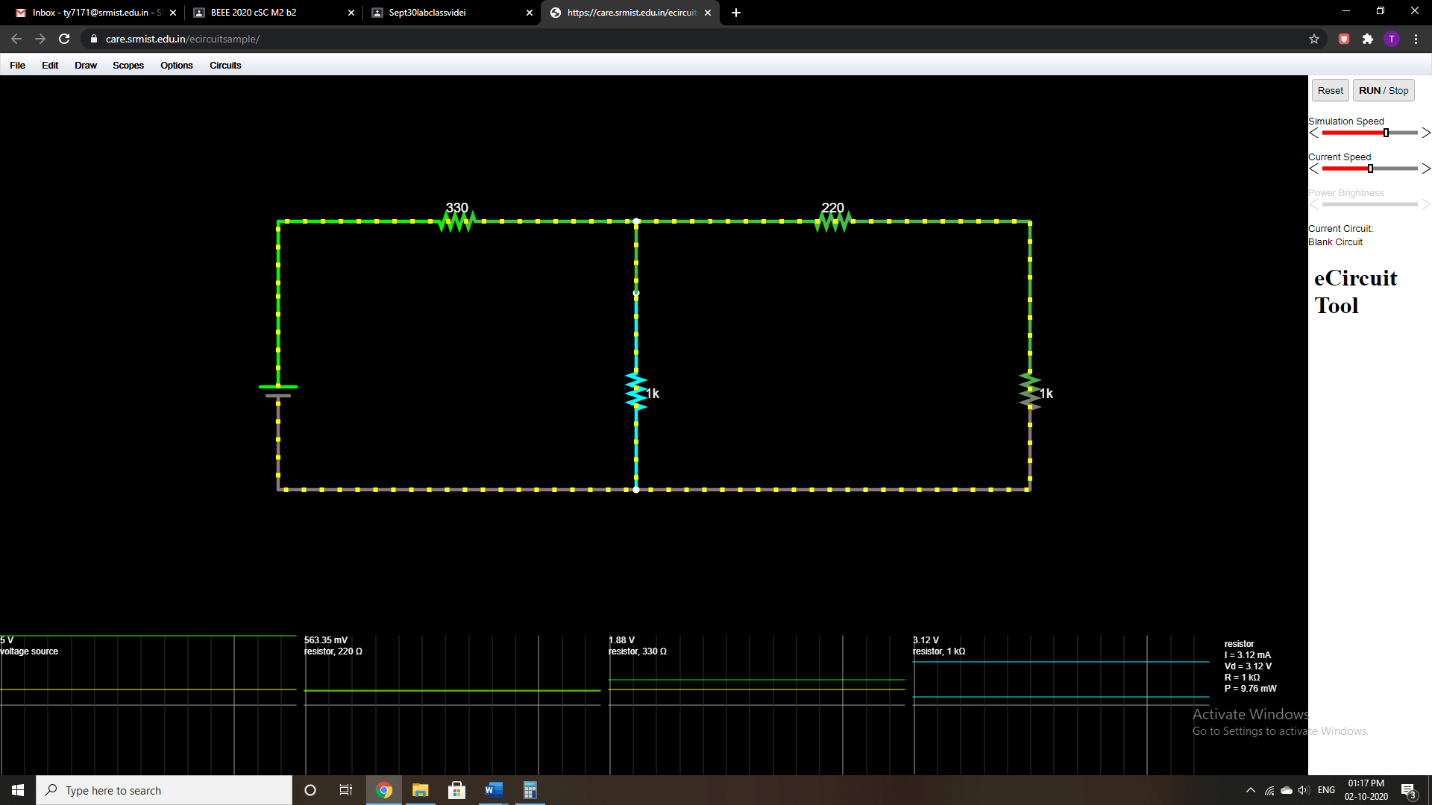
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**Result :** *Thus, Kirchhoff’s Current law & Kirchhoff’s Voltage law for the given circuit is proved.*

***Screenshots of E-Circuits with input voltage of 5V.***

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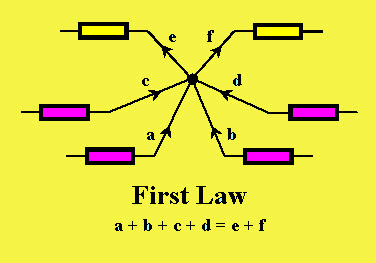




**POST LAB QUESTIONS**

1. **Illustrate KCL and KVL.**

**Ans :-** *KCL or Kirchhoff’s current law or Kirchhoff’s first law states that the total current in a closed circuit, the entering current at node is equal to the current leaving at the node or the algebraic sum of current at node in an electronic circuit is equal to zero.*

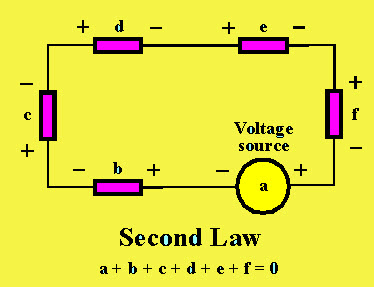
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*KIRCHHOFF’S CURRENT LAW*

*In the above diagram, the currents are denoted with a,b,c,d and e. According to the KCL law, the entering currents are a,b,c,d and the leaving currents are e and f with negative value.*

*Generally in an electrical circuit, the term node refers to a junction or connection of*[*multiple components or elements*](https://www.elprocus.com/basic-components-used-electronics-electrical/)*or current carrying lanes like components and cables. In a closed circuit, the current flow any in or out of a node lane must exist. This law is used to analyze parallel circuits.*

*KVL or Kirchhoff’s voltage law or Kirchhoffs second law states that, the algebraic sum of the voltage in a closed circuit is equal to zero or the algebraic sum of the voltage at node is equal to zero.*

**

*KIRCHHOFF’S VOLTAGE LAW*

*This law deals with voltage. For instance, the above circuit is explained. A voltage source ‘a’ is connected with five passive components, namely b, c, d, e, f having voltage differences across them. Arithmetically, the voltage difference between these components add together because these components are connected in series. According to the KVL law, the voltage across the passive components in a circuit is always equal & opposite to the voltage source. Hence, the sum of the voltage differences across all the elements in a circuit is always zero.*

1. **Express the limitations of Ohm’s law?**

**Ans :- *Following are the limitations of Ohm’s Law:***

*Ohm’s law is not applicable for unilateral electrical elements like diodes and transistors as they allow the current to flow through in one direction only.*

*For non-linear electrical elements with parameters like capacitance, resistance etc the voltage and current won’t be constant with respect to time making it difficult to use Ohm’s law.*

1. **What is the practical application of Kirchhoff’s law?**

**Ans :- *The application of Kirchhoff rule in daily life are:***

*The current of distribution in the various branches of a circuit can easily be found out by applying the Kirchhoff Current law at the different junction points and the nodes in the circuit.*

*After that Kirchhoff Voltage law is applied to each possible loop in the circuit generates algebraic equation for every loop.* *Kirchhoff's Laws are useful in understanding the transfer of energy through an electric circuit. They are also valuable in analyzing electric circuits.*

1. **Compare series and parallel circuits.**

**Ans :-**

|  |  |
| --- | --- |
| ***Difference Between Series and Parallel Circuits*** | |
| ***Series*** | ***Parallel*** |
| *The same amount of current flows through all the components.* | *The current flowing through each component combines to form the current flow through the source.* |
| *In an electrical circuit, components are arranged in a line.* | *In an electrical circuit, components are arranged parallel to each other.* |
| *When resistors are put in a series circuit, the voltage across each resistor is different even though the current flow is the same through all of them.* | *When resistors are put in a parallel circuit, the voltage across each of the resistors is the same. And even the polarities are the same.* |
| *If one component breaks down, the whole circuit will burn out.* | *Other components will function even if one component breaks down, each has its own independent circuit.* |
| *If Vt is the total voltage then it is equal to V1+V2+V3* | *If Vt is the total voltage then it is equal to V1=V2=V3* |

1. **What is the difference between series and parallel connection of batteries?**

**Ans :-***In a series connection, batteries of like voltage are connected to increase the voltage of the overall assembly. The positive terminal of the first battery is connected to the negative terminal of the second battery and so on, until the desired voltage is reached. The final voltage is the sum of all battery voltages added together.*

*In a parallel connection, batteries of like voltages and capacities are connected to increase the capacity of the overall assembly. The positive terminals of all batteries are connected together, or to a common conductor, and all negative terminals are connected in the same manner. The final voltage remains unchanged while the capacity of the assembly is the sum of the capacities of the individual batteries of this connection.*